Sierra Components, Inc.

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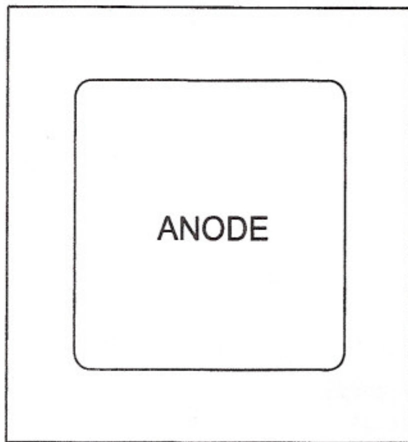
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	18 X 18 MILS
Die Thickness	7.5 MILS
Anode Bonding Pad Area	11 X 11 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 14,000Å

GEOMETRY



BACKSIDE CATHODE R0

GROSS DIE PER 4 INCH WAFER
36,600

PRINCIPAL DEVICE TYPES
CMPZ5235B
THRU
CMPZ5261B

APPROVED BY:MG	DIE SIZE :18 x 18 Mils	DATE: 2/1/10
MFG:Central Semi	THICKNESS:	P/N:CMPZ5239B